SIDDHARTH INSTITUTE OF ENGINEERING AND TECHNOLOGY :: PUTTUR
(AUTONOMOUS)
Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK

Subject with Code :AICD(16EC5702)

Course & Branch: M.Tech – (VLSI) **Year & Sem:** I-M.Tech & I-Sem

UNIT –I
INTEGRATED DEVICES AND MODELLING AND CURRENT MIRROR

1. a) Explain in detail about MOS transistors modeling in saturation and cutoff in highfrequency equivalent circuit. [5M]
   b) Explain the advantages of MOS technology over bipolar technology and why MOS devices gained predominance over bipolar devices. [5M]
2. a) Draw the small signal model for the common source stage and derive the equations for small signal and also explain how to maximize the gain. [5M]
   b) Discuss the frequency response of high output impedance current mirror circuit. [5M]
3. a) Design simple CMOS current mirror circuit and explain its operation [5M]
   b) Explain about the source follower with current mirror to supply bias current. [5M]
4. a)Explain the operation of simple CMOS current mirror [5M]
   b) Explain the basic electrical properties of MOS circuit in non-saturated region and saturatedregion. [5M]
5. a) Draw the MOS transistor characteristics for enhancement mode and depletion mode. [5M]
   b)What are the deficiencies of MOS technology? How they can it be overcome. [5M]
6. a) Explain briefly large signal modeling for BJT with basic current mirrors. [5M]
   b) Discuss the frequency response of single stage BJT amplifiers. [5M]
7. a) Explain the effect of threshold voltage on MOSFET current equations. [5M]
   b) Explain the advantages of MOS technology over bipolar technology and why MOS devices gained predominance over bipolar devices. [5M]
8. a)Draw the structure of a MOS device and explain how it works, with the help of characteristics. [5M]
   b) What are the deficiencies of MOS technology? How they can be overcome. [5M]

9. a) Explain in detail about MOS transistors modeling in saturation and cut off in high frequencyequivalent circuit. [5M]

   b) Discuss in detail about large signal and small signal modeling for BJT. [5M]

10. a) Explain the effect of threshold voltage on MOSFET current equations. [5M]

    b) Explain briefly large signal modeling for BJT with basic current mirrors. [5M]

UNIT –II
OPERATIONAL AMPLIFIER DESIGN AND COMPENSENSATION

1.a) Discuss the various short channel effects in MOS devices. [5M]

b) Draw the noise model of a source follower with necessary equations.[5M] 2.a) Explain why common mode feedback is required. [5M]

b) Explain charge injection error. [5M]

3.a) Draw the circuit diagram of common source stage with active load and find its gain.[5M]

b) Explain how the folded-cascode improves the voltage gain. [5M]

4.a)Explain latched comparators. [5M]

b)Explain the design considerations of Bi-CMOS comparator.

5.a)Explain about advanced current mirror circuits. [5M]

b) Explain about two stage CMOS operational amplifier. [5M]

6 Explain about:

a)Bi-CMOS comparator. [5M]

b) Fully differential amplifier.[5M]

7.a) Explain the terms stability, frequency compensation and phase margin in op-amp [5M]

b) Explain what is meant by dominant pole compensation in operational amplifiers. [5M]

8.a) Explain in detail about current feedback OP-amplifier. [5M]

b) Explain about two stage CMOS operational amplifier [5M]

9.a)Discuss about current mirror op-amp. [5M]

b) Explain about common-mode feedback circuit [5M]

10.Discuss the operation of op-amps with current mirror load. [10M]

UNIT –III
SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUIT-I & II

1. a) Draw a neat figure and explain the basic operation of Bi-CMOS sample and hold circuit. [5M]
   b) What is the function of a first order filter in sample and hold circuit. [5M]
2. a) Explain the correlated double sampling techniques with suitable example. [5M]
   b) Explain about folded cascade operational amplifier operation with circuit diagram. [5M]
3. Discuss in detail about

a)CMOS. [5M]

b)Bi-CMOS sample and hold circuit.[5M]

4. Discuss in detail about correlated double sampling techniques. [10M]
5. a) Give the schematic of a simple sample and hold circuit using a MOS switch.[5M]
   b) Explain what is meant by channel charge injection error and how it is minimized. [5M]
6. a)Explain MOS sample and hold circuit [5M]
   b)What is the need for double sampling techniques. [5M]
7. a)Explain the function of folding and pipelining. [5M]
   b) Draw a neat figure and explain the operation of a switched capacitor circuit [5M]
8. Explain what is meant by correlated double sampling (CDS) technique. What are the advantages of correlated double sampling techniques. [10M]
9. Illustrate with an example how CDS techniques can be used to minimize offsets, 1/f noise and other errors in switched capacitor circuits. [10M]

10.a) Explain about Switched capacitor gain circuit.[5M]

b)Design about Biquard filter. [5M]

UNIT-IV
DATA CONVERTERS

1. a) Explain the operation of over sampling A/D converter. [5M]
   b) Explain briefly about Hybrid converter. [5M]
2. a) Differentiate interpolation and decimation. [5M]
   b) Explain the design procedure for integrates A/D converters. [5M]
3. a) Folding and pipelined A/D converters. [5M]
   b) Define the terms resolution, offset and gain errors, integral linearity error an differential non linearity error in respect of Nyquist D/A converters. [5M]
4. a) Draw the schematic of 4 bit resistor based binary weighted D/A converter and explain itoperation. What are the advantages of binary weighted converters?
   b) With the help of a neat diagram, explain the working of a successive approximation ADC. [5M]
5. a) Explain the working of a Hybrid DAC. [5M]
   b) Explain the function of folding and pipelining. [5M]
6. a) Explain the parameters quantization noise and Nyquist rate with respect to an ideal D/A &A/D converters. [5M]
   b) Write briefly about:
   i. Binary scaled converters. [3M]
   ii.Pipelined A/D converters. [2M]
7. a) Explain the design procedure for successive approximation type DAC. [5M]
   b) Explain about Cyclic flash type ADC. [5M]
8. a) Explain in detail about Ideal D/A & A/D converters. [5M]
   b) Explain in detail about Nyquist rate D/A converters. [5M]
9. a) Describe the working of a binary scaled DAC. [5M]
   b) Explain about Twostep ADC. [5M]
10. a) Explain about interpolating A/D converters. [5M]
    b) Explain about Time interleaved A/D converters. [5M]

UNIT –V
OVER SAMPLING CONVERTERS AND FILTERS

1. a) Write about Digital decimation filter. [5M]
   b) Write about over sampling without noise shaping. [5M]
2. Write explanatory notes on:
   a)Over sampling with Noise shaping. [5M]
   b)Continuous time filters. [5M]
3. Discuss in detail about band pass over sampling converter [10M]
4. Write about over sampling advantages and disadvantages. [10M]
5. a) Define the term over sampling ratio (OSR) in data converters. Explain how oversampling improves the signal to noise ratio of a data converter. [5M]
   b) Digital decimation filter. [5M]
6. a)Explain the structure of a first order noise shaped sigma delta modulator. [5M]
   b) How does noise shaping improve the signal to noise ratio. [5M]
7. Discuss in detail about over sampling with and without noise shaping. [10M]
8. a) Explain about practical considerations for stability. [5M]
   b) Discuss about linearity of two –level converters. [5M]
9. a) Explain about multi bit oversampling converters. [5M]
   b) Explain about dynamic matched current sources in a D/A converter. [5M]
10. a) Discuss about third-order A/D design example. [5M]
    b) Explain digital calibration A/D converter.[5M]

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Prepared by: **M .SHOBHA**